SC11100ZP

#15 Appeal Brief A Ford 12/10/02

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s):	William C. Peatman Eric S. Johnson Adolfo C. Reyes	Atty Docket No.	SC11100ZP
Serial No.:	**09/592,349**	Group Art Unit:	**2814**
Filed:	06/12/2000	Examiner:	**D. Wille**

TITLE: **METHOD OF MANUFACTURING A SEMICONDUCTOR COMPONENT AND SEMICONDUCTOR COMPONENT THEREOF**

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class mail in an envelope addressed to: Commissioner of Patents and Trademarks; Washington, DC 20231, on:

Date: 11-26-02 **By:** [signature]

Printed Name: Sandy Hartway

BRIEF ON APPEAL

Honorable Commissioner of Patents and Trademarks,
Washington, D.C. 20231

SIR:

Please consider the following Brief on Appeal for the above identified patent application assigned to Motorola, Inc.

I. REAL PARTY IN INTEREST

The subject application is assigned to Motorola, Inc. – the real party in interest.

II. RELATED APPEALS AND INTERFERENCES

To Appellants' knowledge, there are no related appeals or interferences.

III. STATUS OF CLAIMS

1. A copy of claims **1**, **2** and **4-21** are provided in Appendix A; the claims corresponding to those on appeal after entry of the Amendment pursuant to 37 CFR §1.116 dated August 22, 2002 in response to the Action dated April 02, 2002.

2. Claims **1**, **4-16**, **20** and **21** stand rejected under 35 U.S.C. §103(a) as purportedly unpatentable over U.S. Patent No. 5,895,929 to Abrokwah *et al.* in view of JP Patent No. 401124267A to Kimura.

3. Claims **2**, **3** and **19** stand rejected under 35 U.S.C. §103(a) as purportedly unpatentable over U.S. Patent No. 5,895,929 to Abrokwah *et al.* in view of JP Patent No. 401124267A to Kimura and in further view of U.S. Patent No. 5,614,739 to Abrokwah *et al.*

4. Claims **7** and **18** stand rejected under 35 U.S.C. §103(a) as purportedly unpatentable over U.S. Patent No. 5,895,929 to Abrokwah *et al.* in view of U.S. Patent No. 5,937,285 to Abrokwah.

IV. STATUS OF AMENDMENTS FILED AFTER FINAL REJECTION

Applicants filed an Amendment pursuant to 37 CFR §1.116 dated August 22, 2002 in response to the final Action dated April 02, 2002. There has been no correspondence or other indication that the Examiner intends to refuse entry of the Amendment. The Amendment has been offered for the express purpose of presenting claims **1**, **2**, **16** and **19** in better form for consideration on Appeal inasmuch as their amendment serves to

substantially reduce the number of material issues in dispute and in the hopes of promoting prosecutorial, administrative and judicial economy. Specifically, the amendments presented therein eliminate consideration as to whether the thickness of the GaAs layer may be less than 6 nm and, if presented earlier, would have substantially reduced the scope of the prior art search. Accordingly, the issues are more clearly defined on Appeal with no requirement for further searching on the part of the Examiner.

V. SUMMARY OF INVENTION

A representative and exemplary embodiment of the present invention is directed to a method of manufacturing a semiconductor component, as generally depicted if Figures **1** and **2**, by providing a substrate **110** with a surface **119**, providing a layer **120** of undoped gallium arsenide having a thickness of at least 6 nm over the surface **119** of the substrate **110**, forming a gate contact **210** over a first portion of the layer **120**, and removing a second portion of the layer **120**, wherein the remaining first portion of layer **120** does not substantially extend beyond the horizontal profile of the gate contact **210**.

VI. ISSUES

Whether procedural fairness has been extended to Applicants in the prosecution of the subject Application as well as in consideration of Applicants' previously submitted arguments on the merits;

Whether any combination of the references proposed by the Examiner effectively establish a *prima facie* basis for obviousness under 35 U.S.C. §103(a); and more specifically,

Whether claims **1**, **4-16**, **20** and **21** are obvious over U.S. Patent No. 5,895,929 to Abrokwah *et al.* in view of JP Patent No. 401124267A to Kimura; whether claims **2**, **3** and **19** are obvious over U.S. Patent No.

5,895,929 to Abrokwah *et al.* in view of JP Patent No. 401124267A to Kimura and in further view of U.S. Patent No. 5,614,739 to Abrokwah *et al.*; and whether claims **7** and **18** are obvious over U.S. Patent No. 5,895,929 to Abrokwah *et al.* in view of U.S. Patent No. 5,937,285 to Abrokwah.

VII. GROUPING OF CLAIMS

Appellants offer no other grouping of claims.

VIII. ARGUMENTS

Claims **1**, **4-16**, **20** and **21** stand rejected under 35 U.S.C. §103(a) as purportedly unpatentable over U.S. Patent No. 5,895,929 to Abrokwah *et al.* in view of Kimura. The Examiner suggests that, with respect to claims **1**, **4-13**, **15**, **16** and **20**, Abrokwah '929 discloses a HFET with a substrate 10 of GaAs, with AlGaAs intermediate layers, with layer 16 of GaAs, delta doped layer 22, InGaAs channel layer 23, AlGaAs layer 24 and GaAs cap layer 25. The Examiner further suggests that Abrokwah '929 discloses a gate contact 30 having sidewalls 35 with the layer 25 partly removed. While the Examiner admits that Abrokwah '929 does not show layer 22 as comprising GaAs, the Examiner suggests that it would have been obvious to form layer 22 with GaAs in order to demonstrate bandgap discontinuity. The Examiner further suggests that since layer 22 is delta doped, layer 22 would have some undoped material on either face. The Examiner also proposes that implantation in the Abrokwah '929 disclosure is performed before layer 25 is removed. The Examiner further suggests that Kimura discloses a FET where an *i*-GaAs gate layer demonstrates width on the order of the gate contact. Finally, the Examiner proposes that it would have been obvious to apply the Kimura technique to the Abrokwah '929 device "for the advantage shown".

As a preliminary matter, Applicants are without notice and/or understanding as to what "advantage" the Examiner intended to make reference to in the correspondence dated April 02, 2002. The Examiner references "the

advantage shown", ostensibly in support of the synthetic combination of Abrokwah '929 with Kimura; however, Applicants are wholly unable to identify or otherwise ascertain any "advantage" having been motivated (much less demonstrated) or otherwise indicated in the disclosures of either Kimura or Abrokwah '929 – or, for that matter, in the combination of the same. Applicants asserted the argument that the Examiner "cannot simply reach conclusions based on [his] own understanding or experience – or on [his] assessment of what would be basic knowledge or common sense"; rather, the Examiner must point to some concrete evidence in the record in support his findings of obviousness. *See, In Re Zurko*, 258 F.3d 1379 (2001) where the court found conclusions of obviousness lacking substantial evidentiary support to constitute reversible error on the part of the Office.

Moreover, to the extent that the Abrokwah '929 reference was erroneously identified and combined with the Kimura reference, as the Examiner has previously admitted, and inasmuch as the proper reference should have been the Abrokwah '739, Applicants respectfully requested that the Examiner withdraw the finality of the then pending Action so that Applicants' could be extended fair procedural opportunity to formally respond to the Examiner's concerns as they related to the correct reference. The Examiner was unresponsive to Applicants' request to remove the finality of the April 02, 2002 Action.

Notwithstanding the preceding, Applicants respectfully traversed the rejections as applied to the erroneous Abrokwah '929 reference. Applicants requested that the Examiner consider that in order to establish a *prima facie* case of obviousness under §103, three basic criteria must be met under MPEP 2143: (1) there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings; (2) there must be a reasonable expectation of success; and (3) the prior art reference (or references when combined) must teach or suggest **all of the claim limitations** (*emphasis added*).

With respect to the first requirement as it related *inter alia* to the rejection of independent claims **1** and **16**, the Action failed to provide a reasoned basis for the suggestion or motivation to modify or combine the disclosure of Abrokwah '929 with that of Kimura and/or any other teaching or reference of record. *See, for example, In re Lee*, 277 F.3d 1338, 1343 (Fed. Cir. 2002), where the Examiner's obligation to explain the reasons one of ordinary skill in the art would have been motivated to select the references and to combine them to render the claimed invention is described. The factual question of motivation is material to patentability and cannot be resolved based on subjective belief and unknown authority. *Id.* at 1344. Obviousness cannot be established by combining the teachings of the prior art to produce the claimed invention, absent some teaching or suggestion supporting the combination. Under section 103, teachings of references may be combined only if there is some suggestion or incentive to do so. *See, ACS Hospital Systems, Inc. v. Montefiore Hospital*, 732 F.2d 1572 at 1577. The critical inquiry is whether there is something in the prior art as a whole to suggest the desirability, and thus the obviousness, of making the combination. *See, Fromson v. Advance Offset Plate*, 755 F.2d 1549 at 1556.

The Examiner asserts that it would have been obvious to make the proposed combinations to arrive at the Appellants' claimed invention. Appellants' respectfully submit that these statements are unsupported assertions expressing *conclusions* and as such are *not* reasons for rejection under 35 U.S.C. § 103(a). Moreover, the test for obviousness must come from, or at least be compatible with, the requirements of 35 U.S.C. § 103(a), stating that: " . . . if the differences between the subject matter sought to be patented and the prior art are such that ***the subject matter as a whole*** would have been obvious . . ." (emphasis added; 35 U.S.C. § 103(a)). The Action's unsupported assertions at most address obviousness of a *difference* between the claimed subject matter and the prior art, and not obviousness of the *claimed subject matter as a whole*, as required by the plain language of 35 U.S.C. § 103(a). Accordingly, the rejection in question may only be construed to have been based upon a hindsight reconstruction enlightened by Appellants' own disclosure. As the CAFC stated in *W.L Gore Associates, Inc. v. Garlock, Inc.* (220 USPQ 303, 312-13 (Fed. Cir. 1983)):

> To imbue one of ordinary skill in the art with knowledge of the invention in suit, where no prior art reference or references of record convey or suggest that knowledge, is to fall victim to the insidious effect of a hindsight syndrome wherein that which only the inventor taught is used against its teacher.

To the extent that such a suggestion or motivation was not identified, under the second requirement, there could accordingly be no reasonable expectation of success. Any expectation of success could therefore only be unreasonable, at best. Moreover, an affidavit previously submitted in accordance with Rule 1.132 by Jonathan K. Abrokwah (the patentee whose art was cited by the Examiner in purported support of all of the Examiner's rejections) indicated that the regime at and above an undoped gallium arsenide thickness of 6 nm would not have been expected to even work! This affidavit is presented herein for the Board's review and consideration as Exhibit A.

The Examiner has failed to show either a suggestion in the art or a compelling motivation based on sound scientific principles to combine the references and therefore the rejection under 35 U.S.C. § 103(a) is improper and should be withdrawn. Appellants respectfully submit that there is no suggestion to combine the references, or in the alternative, if they could be properly combined, do not lead to the Appellants' invention.

Even if the Abrokwah '929 disclosure (or any other Abrokwah disclosure, to include Abrokwah '739) were combined with that of Kimura and/or any other reference, knowledge or teaching of record, such a combination would not lead a person skilled in the art to develop Applicants' invention; namely, a method of manufacturing a semiconductor component with the described layer of undoped gallium arsenide having "a thickness of **at least six to approximately twelve nanometers**". (*See* claim **1** as amended; *emphasis added*).

It is respectfully pointed out that the limitation of "at least six to approximately twelve nanometers" is not found, suggested or otherwise motivated in the cited art and that functional claim language must be considered in evaluating a claim relative to the prior art. *See, Lewmar Marine, Inc. v. Barient, Inc.*, 827 F.2d 744 (Fed. Cir. 1987); and *Raytheon Co. v. Roper Corp.*, 724 F.2d 951 (Fed. Cir. 1983). The Office is not permitted to ignore the results and advantages produced by claimed subject matter, of which the prior art is devoid, simply because the claim limitations are similar to that otherwise found in the prior art. *See, for example, Diversitech Corp. v. Century Steps, Inc.*, 850 F.2d 675 (Fed. Cir. 1988); *In re Chupp*, 816 F.2d 643 (Fed. Cir. 1987); *Fromson v. Advanced Offset Plate*, 755 F.2d 1549 (Fed. Cir. 1985); *In re Piasecki*, 745 F.2d 1468 (Fed. Cir. 1984); and *Carl Schenck, A.G. v. Nortron Corp.*, 713 F.2d 782 (Fed. Cir. 1983).

It is important to note here that in previous telephonic correspondence with the Examiner, Applicants pointed out that the Abrokwah '929 reference was malformed in the combinatorial syntheses corresponding to the §103(a) rejections in the original action. The Examiner agreed and conceded that the proper reference should have been Abrokwah '739. When Applicants' submitted proposed amendments to further limit the *i*-GaAs thickness range from "approximately 3 nm to 12 nm" to "at least 6 nm to approximately 12 nm", the Examiner suggested that amendment of the claimed range to recite "at least 7 nm to approximately 12 nm" would be provisionally allowable in view of the Abrokwah '739 disclosure of a preferred embodiment having an *i*-GaAs thickness of "less than approximately fifty angstroms" (*i.e.*, 5 nm) at col. 2, lines 20-24. When Applicants' requested an explanation as to the significance the thickness of 7 nm carried in the Examiner's consideration of provisional allowance, the Examiner was unable to identify where any clear cut-off might be made. However, when this issue was further probed by Applicants', the Examiner indicated that neither 6.25 nm, 6.50 nm nor 6.75 nm would be sufficient, but that the examiner would allow the case if Applicants amended the range to "at least 7.0 nm". Applicants' communicated their belief that such an determination, unsubstantiated with a reasonable basis for presenting a cut-off at 7.0 nm, was quite arbitrary and would not likely be favorably viewed on Appeal. At this point,

the Examiner agreed that the Board would probably not uphold his decision, but that his decision would nevertheless remain in force at that point in prosecution. Applicants' attempted to submit further argument and evidence that the Abrokwah '739 reference only teaches or otherwise motivates operational GaAs thicknesses in the range of 5 nm and less and that Applicants' proposed range would suggest thickness in the range of at least greater than 6 nm. Applicants' also proffered argument by way of affidavit from Jonathan Abrokwah himself that he was not motivated to look beyond 5 nm because he didn't think it would work and the fact that it did work was an dramatically unexpected result! The Examiner remained unpersuaded without indication that secondary indicia of non-obviousness with respect to the submitted evidence of unexpected results was even considered. The Examiner then proposed that continuation of the case would not likely advance prosecution, leaving Applicants with no alternative other than Appeal.

Appellants' respectfully submit that independent claims **1** and **16** as amended clearly distinguish over the cited art. In particular, neither abrokwah '929, Abrokwah '739, Abrokway '285 nor Kimua, taken individually or in combination, disclose or teach a method of manufacturing a semiconductor component with the described layer of undoped gallium arsenide having a thickness of at least six to approximately twelve nanometers. Abrokwah '929, Abrokwah '739, Abrokway '285 nor Kimua, individually or in combination, do not contain at least this feature of any of the Appellants' claims. Accordingly, they do not include, suggest or otherwise motivate all of the elements of Appellants' independent claims **1** and **16**, and therefore cannot be construed to render Appellants' independent claims obvious as the Examiner suggests. Therefore, Appellants' respectfully submit that the rejection is improper and should be withdrawn.

Notwithstanding the recitation of novel elements in each of claims **4-13**, **15** and **20**, inasmuch as these claims variously depend from and incorporate all of the limitations of their corresponding independent claims **1** and **16** as amended, dependent claims **4-13**, **15** and **20** are similarly allowable over the art of record.

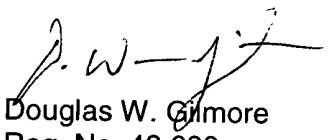
Notwithstanding the recitation of novel elements in claims **14** and **21**, inasmuch as these claims depend from and incorporate all of the limitations of independent claim **1** as amended and dependent claim **20** (which depends from independent claim **16** as amended), dependent claims **14** and **21** are similarly allowable over the art of record.

Notwithstanding the recitation of novel elements in claim **19**, inasmuch as this claim depends from and incorporates all of the limitations of independent claim **16** as amended, dependent claim **19** is similarly allowable over Abrokwah '929 in combination with Kimura in view of Abrokwah '739.

Notwithstanding the recitation of novel elements in claims **17** and **18**, inasmuch as these claims depend from and incorporate all of the limitations of independent claim **16** as amended, dependent claims **17** and **18** are similarly allowable over Abrokwah '929 in view of Abrokwah '285.

Appellants therefore respectfully request reversal of the final rejection and the allowance of the subject application.

Respectfully submitted,



Douglas W. Gilmore
Reg. No. 48,690

Dated: November 25, 2002

Motorola, Inc.
Corporate Law Department
Mail Drop 56-238
3102 North 56th Street
Phoenix, AZ 85018-6697

Douglas W. Gilmore
Attorney for Applicants
Tel 602.952.3482
doug.gilmore@motorola.com

APPENDIX A

1. (twice amended) A method of manufacturing a semiconductor component comprising:

providing a substrate with a surface;

providing a layer comprising a thickness of at least six to approximately twelve nanometers of undoped gallium arsenide over the surface of the substrate;

forming a gate contact over a first portion of the layer; and

removing a second portion of the layer to expose a portion of the surface of the substrate, wherein the remaining first portion of said layer does not substantially extend beyond the horizontal profile of said gate contact.

2. (amended) The method of claim 1 wherein:

said layer comprises a thickness of at least six to approximately nine nanometers of undoped gallium arsenide.

4. The method of claim 1 wherein:

forming the gate contact further comprises exposing the second portion of the layer.

5. The method of claim 1 wherein:

removing the second portion of the layer exposes a portion of the substrate.

6. The method of claim 1 further comprising:

implanting source and drain regions into the substrate after removing the second portion of the layer.

7. The method of claim 1 further comprising:

implanting source and drain regions into the substrate before removing the second portion of the layer.

8. The method of claim 1 further comprising:

forming a spacer adjacent to the gate contact after removing the second portion of the layer.

9. The method of claim 1 further comprising:

forming a spacer adjacent to the gate contact before removing the second portion of the layer.

10. The method of claim 9 further comprising:

keeping a third portion of the layer underneath the spacer after removing the second portion of the layer.

11. The method of claim 1 wherein:

providing the substrate further comprises providing a delta-doped, heteroepitaxial semiconductor structure for the substrate.

12. The method of claim 1 wherein:

providing the substrate further comprises:

providing a support layer;

providing a buffer layer overlying the support layer;

providing a doping layer overlying the buffer layer;

providing a spacer layer overlying the doping layer;

providing a channel layer overlying the spacer layer; and

providing a barrier layer overlying the channel layer.

13. The method of claim **1** wherein:

forming the gate contact further comprises:

forming the gate contact on the layer.

14. The method of claim **1** further comprising:

implanting source and drain regions into the substrate;

annealing the source and drain regions after removing the second portion of the layer; and

forming source and drain contacts over the source and drain regions after removing the second portion of the layer.

15. The method of claim **1** wherein:

removing the second portion of the layer further comprises keeping the first portion of the layer underneath the gate contact; and

removing the second portion of the layer further comprises keeping the first portion of the layer undoped.

16. (twice amended) A method of manufacturing a semiconductor component comprising:

providing a delta-doped, heteroepitaxial semiconductor substrate with a surface, the delta-doped, heteroepitaxial semiconductor substrate comprising:

a support layer comprised of semi-insulating gallium arsenide;

a buffer layer comprised of undoped gallium arsenide overlying the support layer;

a doping layer delta-doped with silicon and overlying the buffer layer;

a spacer layer comprised of undoped gallium arsenide and overlying the doping layer;

a channel layer comprised of indium gallium arsenide and overlying the spacer layer; and

a barrier layer comprised of aluminum gallium arsenide and overlying the channel layer, the barrier layer forming the surface for the delta-doped, heteroepitaxial semiconductor substrate;

providing an undoped gallium arsenide capping layer having a thickness of at least six to approximately twelve nanometers and overlying the surface of the delta-doped, heteroepitaxial semiconductor substrate;

forming a gate contact over the undoped gallium arsenide capping layer, the gate contact covering a first portion of the undoped gallium arsenide capping layer and absent over a second portion of the undoped gallium arsenide capping layer;

removing the second portion of the undoped gallium arsenide capping layer after forming the gate contact to expose a portion of the surface of the delta-doped, heteroepitaxial semiconductor substrate, wherein the remaining first portion of said undoped gallium arsenide capping layer does not substantially extend beyond the horizontal profile of said gate contact;

forming a spacer adjacent to the gate contact;

forming source and drain regions in the delta-doped, heteroepitaxial semiconductor substrate; and

forming source and drain contacts over the source and drain regions after removing the second portion of the undoped gallium arsenide capping layer.

17. The method of claim **16** wherein:

forming the source and drain regions further comprises implanting the source and drain regions into the delta-doped, heteroepitaxial semiconductor substrate after removing the second portion of the undoped gallium arsenide capping layer; and

forming the spacer further comprises forming a multi-layered spacer adjacent to the gate contact after removing the second portion of the undoped gallium arsenide capping layer.

18. The method of claim **16** further comprising:

forming the source and drain regions further comprises implanting source and drain regions into the delta-doped, heteroepitaxial semiconductor substrate before removing the second portion of the undoped gallium arsenide capping layer;

forming the spacer further comprises forming a multi-layered spacer adjacent to the gate contact before removing the second portion of the undoped gallium arsenide capping layer; and

keeping a third portion of the undoped gallium arsenide capping layer underneath the multi-layered spacer after removing the second portion of the undoped gallium arsenide capping layer.

19. (amended) The method of claim **16** wherein:

providing the undoped gallium arsenide capping layer further comprises providing the undoped gallium arsenide layer with a thickness of at least six to approximately nine nanometers.

20. The method of claim **16** wherein:

providing the delta-doped, heteroepitaxial semiconductor substrate further comprises:

providing the buffer layer on the support layer and consisting essentially of gallium arsenide;

providing the doping layer on the buffer layer and consisting essentially of silicon and gallium arsenide;

providing the spacer layer on the doping layer and consisting essentially of gallium arsenide;

providing the channel layer on the spacer layer and consisting essentially of indium gallium arsenide; and

providing the barrier layer on the channel layer and consisting essentially of aluminum gallium arsenide;

providing the undoped gallium arsenide capping layer further comprises:

providing the undoped gallium arsenide capping layer on the barrier layer;

forming the gate contact further comprises:

forming the gate contact on the first portion of the undoped gallium arsenide capping layer; and

removing the second portion of the undoped gallium arsenide capping layer further comprises:

removing the second portion of the undoped gallium arsenide capping layer to expose a portion of the barrier layer.

21. The method of claim **20** further comprising:

annealing the source and drain regions after removing the second portion of the undoped gallium arsenide capping layer,

wherein:

providing the undoped gallium arsenide capping layer further comprises providing the undoped gallium arsenide capping layer with a thickness of approximately six to nine nanometers.

SC11100ZP
patent application

EXHIBIT A

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s):	William C. Peatman Eric S. Johnson Adolfo C. Reyes	Atty Docket No.	SC11100ZP
Serial No.:	**09/592,349**	Group Art Unit:	**2814**
Filed:	06/12/2000	Examiner:	**D. Wille**
TITLE:	**METHOD OF MANUFACTURING A SEMICONDUCTOR COMPONENT AND SEMICONDUCTOR COMPONENT THEREOF**		

FAX TRANSMISSION CERTIFICATE

I hereby certify that this correspondence, pursuant to 37 C.F.R. §1.8, is being submitted via facsimilie transmission to The United States Patent and Trademark Office on:

Date: August 23, 2002 **By:** [signature]

Printed Name: SALLY HARTWAY

AFFIDAVIT PURSUANT TO 37 C.F.R. §1.132

Assistant Commissioner of Patents
Washington, D.C. 20231

Dear Assistant Commissioner:

STATE OF ARIZONA)
:
COUNTY OF MARICOPA)

I, Jonathan K. Abrokwah, being duly sworn, depose and say as follows:

I received a Bachelor of Science Degree in Electrical Engineering from the Massachusetts Institute of Technology in 1974. I received a Masters of Science Degree in Electrical Engineering from the Massachusetts Institute of Technology in 1976. I also received a Masters of Science Degree in Materials Science Engineering from the University of Southern California in 1979 and a Doctorate of Science Degree in Electrical Engineering from the University of Southern California in 1979.

I have been employed by Motorola, Inc., Corporate Research Laboratories Sector, since 1990 where I have served in various management and technical capacities, but most recently as Manager for the Advanced Technology Group in the Compound Semiconductor Laboratories of Motorola DDL. Prior to employment with Motorola, my experience and services were retained in various technical and managerial capacities by McDonnell Douglas from 1986 to 1990 and Honeywell from 1979 to 1986. I have, by all accounts, published well over 50 technical papers on semiconductor technology and design. Additionally, I have inventively contributed to 28 issued patents.

When my co-inventors and I developed the inventions corresponding to U.S. Patents No. 5,614,739 and 5,895,929, we were using an undoped GaAs layer having a thickness on the order of 1-5nm; more specifically, in the range of 3-5nm. Neither I nor any of the other inventors of the '929 and '739 patents considered that success could be realized at undoped GaAs thicknesses greater than 5nm. Quite plainly, we didn't think anything greater than 5nm would ever work, which is why the '739 application, for example, teaches layer 17 as being a layer of undoped GaAs that is less than 50 angstroms.

It was our intent in those applications to disclose and teach the benefits of using an undoped GaAs layer less than around 5nm thick. It was also our intent to teach or otherwise suggest that if modifications of the thickness of this layer were to be explored, that those modifications should be made only in order to reduce the thickness of the undoped GaAs layer down from 5nm. To the extent that we did not believe that any thickness above 5nm would work, we certainly did not want to suggest to the reader that thicknesses greater than 5nm could be used. This would not only have obscured our best mode of invention, but also would have been manifestly contrary to the well accepted belief held by those skilled in the art that only GaAs layers less than about 50 angstroms could ever be made to work. We wanted to be clear that an undoped GaAs layer of something less than the upper value of 5nm would be desired.

When I first heard from William Peatman's group that they were operating above 5 nm, I did not believe it. It was an entirely unexpected result that they would have been able to get their invention to work using a GaAs layer with a thickness greater than 5nm. I was even more surprised when I found out that the commercial implementation of Peatman's technology to actual device fabrication using undoped GaAs layers on the order of 7-7.5nm was yielding highly reproducible and favorable production yields.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true. I further declare that these statements are made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful and false statements may jeopardize the validity of the subject patent application or any patent issued thereon.

I further declare that I have received no special compensation or consideration for making this affidavit, nor have I been in any way told, either directly or by implication or inference, by anyone that my employment by Motorola, Inc. or my professional advancement or other matters of personal or professional interest to me depend in any way on whether or not I make this affidavit or the content thereof. I further declare that I make this affidavit of my own free will and choice without any duress or influence of any kind, believing fully in the truth of the statements made by myself herein.

Jonathan K. Abrokwah

Jonathan K. Abrokwah

I, Jeanine L. Thompson, a Notary Public in and for the County and State aforesaid, do hereby certify that Jonathan K. Abrokwah, whose name is subscribed to the foregoing instrument, appeared before me this day in person and acknowledged that he signed, sealed and delivered the said instrument as his free and voluntary act and deed for the uses and purposes therein set forth.

Given under my hand and Notary Seal this 23 day of August, 2002.

Jeanine L. Thompson

JEANINE L THOMPSON
Notary Public - Arizona
Maricopa County
My Comm. Expires Jun 28, 2003

My commission expires on June 28, 2003.

SEAL